

Novel Quantum Structure of an III-V Tunneling Field-Effect Transistor with Source and Channel Heterojunction

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ABSTRACT

In this work, an III-V tunneling field-effect transistor (TFET) with source and channel heterojunctions is proposed and introduced. Proposed structure combine the high tunneling efficiency induced by heterojunction material and the high mobility of III-V material. The III-V TFETs based on either source heterojunction and channel heterojunctions have been intensively researched due to their excellent subthreshold-swing characteristics. However, compared with conventional III-V TFETs, the III-

V TFETs with source and channel heterojunctions have both shorter tunneling distance and two transmission resonances that significantly improve the on-current. The transfer characteristics affected by gate length were also evaluated. The results show that on-current, off-current, and on-current/off-current ratio and subthreshold-swing of III-V TFETs with source and channel heterojunctions are about 10^{-3} A/ μm , 10^{-13} A/ μm , 10^{-10} and 30 mV/decade, respectively.

KEYWORDS: III-V material, source heterojunction, channel heterojunction, Tunneling field-effect transistor (TFET).

Nova estrutura quântica de um transistor de efeito de campo de tunelamento III-V com fonte e canal Heterojunction

RESUMO

Neste trabalho, um transistor de efeito de campo de tunelamento III-V (TFET) com heterojunções de fonte e canal é proposto e introduzido. A estrutura proposta combina a alta eficiência de tunelamento induzida pelo material de heterojunção e a alta mobilidade do material III-V. Os TFETs III-V, baseados em heterojunções de fontes e em heterojunções de canais, têm sido intensamente pesquisados devido às suas excelentes características sub-threshold-swing. No entanto, em comparação com TFETs III-V convencionais, os TFETs III-V com

heterojunções de fonte e de canal têm uma distância de túnel mais curta e duas ressonâncias de transmissão que melhoram significativamente a corrente em andamento. As características de transferência afetadas pelo comprimento da comporta também foram avaliadas. Os resultados mostram que a relação entre corrente, corrente fora de serviço e corrente/corrente fora de limite e TFETs de III-V com heterojunção de fonte e canal são de cerca de 10^{-3} A/ μm , 10^{-13} A/ μm , 10^{-10} e 30 mV/década, respectivamente.

Palavras-Chave: Material III-V, heterojunção de origem, heterojunção de canal, transistor de efeito de campo de tunelização (TFET).

1. INTRODUCTION

Recently, tunneling field-effect transistors (TFETs) are emerged as the most attractive transistor due to their subthreshold-swing, leakage current and transconductance characteristics (Vallett, et al., 2010; Ionescu and Riel, 2011; Marjani, et al., 2016(a); Ameen, et al., 2019; Woo and Kim, 2019). Basically, the TFET is defined as a reverse biased gated p-i-n device, in which the gate controls the band-to-band tunnelling between the source and the drain through modulation of the position of energy bands. In order to occur band-to-band tunnelling in TFETs, several conditions need to be fulfilled (Ameen, et al., 2019; Marjani and Hosseini, 2015(b); Marjani, et al., 2017; Dorostkar and Marjani, 2018). At first, band alignment of source-channel interface and electron and hole layers of channel are formed properly. Second, the electric field is available at source-channel interface to reduce the tunnel barrier height and tunnel distance. Third, the electron and hole wave functions have significant overlap. Forasmuch as the valence band of source is lower than the conduction band of channel in off-state, very little current flows arising from the large tunneling barrier and distance between the source and channel. With applying the gate voltage in on-state, the energy bands of channel come down so that the conduction band of channel is located lower than valence band of source. In this way, the tunneling barrier has been eliminated and the tunneling distance has been shortened. These conditions cause the high electric field at the source-channel interface that forces the electrons to tunnel from the valence band of source to the conduction band of channel through the tunneling window between the source and the channel (Marjani and Hosseini, 2014(a); Marjani and Hosseini, 2014(b); Marjani, et al., 2017; Dorostkar and Marjani, 2018; Horst, et al., 2019).

On the one hand, the silicon-based TFETs have low on-current about 3 decades lower than metal-oxide-semiconductor field-effect transistor (MOSFET) that causes their less competitive in high-performance applications (Sabaghi et al., 2016(a); Sabaghi et al., 2016(b); Dashtbayazi et al., 2015; Das, et al., 2018; Ashita, et al., 2019; Marjani, et al., 2016(b); Marjani, et al., 2016(c)). A number of designs have been proposed to further improve the on-current of the silicon-based TFETs including band-gap engineering (Luisier and Klimeck, 2010; Das, et al., 2015), low band-gap materials (Ganapathi, et al., 2010), high-k dielectric materials (Marjani and Hosseini, 2014(a); Jain et al., 2015; Noor, et al., 2017), source-pocket doping (Chang, et al., 2013; Marjani and Hosseini, 2015(a); Marjani, et al., 2016(b); Marjani, et al., 2017), vertical direction tunneling (Alper, et al., 2018), and extended source (Marjani and Hosseini, 2014(a); Marjani and Hosseini, 2014(b); Marjani, et al., 2017). Another way to overcome this weakness and improve the on-current is replacng silicon with high mobility of III-V material (Marjani, et al., 2016(b); Dorostkar and Marjani, 2018). On the other hand, device geometries have been considered to boosting tunneling probability by employing heterojunction for the tunnel junction to reduce the tunnel barrier height and tunnel distance (Marjani and Hosseini, 2015(a); Marjani and Hosseini, 2015(b); Marjani, et al., 2016(b); Dorostkar and Marjani, 2018).

In this study, an III-V tunneling field-effect transistor with source and channel heterojunctions is proposed and introduced that combine the heterojunction and III-V materials. The simulations of proposed structure were performed by 2D device simulation to meet the high-

performance requirements predicted by the most recent technology roadmap. The model are given in section 2 and the proposed structures are reported in section 3. The results are discussed in section 4 and final conclusion in section 5.

2. MODEL

The carrier continuity equations for electron and hole are defined by (Atlas – Device Simulation Framework., 2018):

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q} \nabla \cdot \vec{J}_n \quad 1$$

$$\frac{\partial p}{\partial t} = G_p - R_p + \frac{1}{q} \nabla \cdot \vec{J}_p \quad 2$$

where n , p , J_n , J_p , G_n , G_p , R_n , R_p and q are the electron concentration, hole concentration, electron current density, hole current density, electrons generation rate, holes generation rate, electrons recombination rate, holes recombination rate and magnitude of the charge on the electron, respectively.

When a high electric field is available at source-channel interface, the carriers tunnel from from the valence band of source into the conduction band of channel. In the other words, an additional carrier is therefore generated in the conduction band that this generation is performed into the right-hand side of the above continuity equations. The nonlocal band-to-band tunneling model calculate a generation rate at each point based solely on the field value nonlocal to that point. Therefore, it need to take into account the spatial variation of the energy bands in order to model the tunneling process more accurately. The net current per unit area is (Atlas – Device Simulation Framework., 2018):

$$J(E) = \frac{q}{\pi \hbar} \iint T(E) [f_l(E + E_T) - f_r(E + E_T)] \rho(E_T) dE dE_T \quad 3$$

where $T(E)$ is the electron tunneling probability, E is longitudinal energy, E_T is the transverse energy and $\rho(E_T)$ is the 2D density of states. f_l and f_r is the Fermi-Dirac function using the quasi Fermi-level on the left and right hand side of the junction, respectively. The equations of the quasi-Fermi level on the left hand side of the junction, the quasi-Fermi level on the right hand side of the junction, 2D density of states and the electron tunneling probability can be defined , respectively, by (Atlas – Device Simulation Framework., 2018):

$$f_l = \left(1 + \exp \left[\frac{E + E_T - E_{Fl}}{KT} \right] \right)^{-1} \quad 4$$

$$f_r = \left(1 + \exp \left[\frac{E + E_T - E_{Fr}}{KT} \right] \right)^{-1} \quad 5$$

$$\rho(E_T) = \frac{\sqrt{m_e m_h}}{2\pi\hbar^2} \quad 6$$

$$T(E) = \exp \left(-2 \int_{x_{start}}^{x_{end}} k(x) dx \right) \quad 7$$

Where k is Boltzmann's constant, T is temperature. m_e is the transverse electron effective mass, m_h is the transverse hole effective mass and \hbar is Planck's constant x_{start} is the start point of the tunneling paths and x_{end} is start and end points of the tunneling paths. $k(x)$ is evanescent wavevector at points and can be calculated as (Atlas – Device Simulation Framework., 2018):

$$k(x) = \frac{k_e k_h}{\sqrt{k_e^2 + k_h^2}} \quad 8$$

where K_e and K_h can be written as (Atlas – Device Simulation Framework., 2018):

$$k_e(x) = \frac{1}{i\hbar} \sqrt{2m_0 m_e(x)(E - E_c(x))} \quad 9$$

$$k_h(x) = \frac{1}{i\hbar} \sqrt{2m_0 m_e(x)(E_v(x) - E)} \quad 10$$

where m_0 is the rest mass of an electron.

In order to calibrate the nonlocal band-to-band tunneling model in the device simulation, should be specified the its values including the rest mass of an electron, electron effective mass and hole effective mass (Atlas – Device Simulation Framework., 2018). These values are 0.32, 0.55 and 0.25 for the electron effective mass, hole effective mass and rest mass of an electron to fit with the experimental data (Marjani and Hosseini, 2014(a); Marjani and Hosseini, 2014(b)). On the other hand, multiple models were included for higher reliability of device simulation results including the Auger recombination, band-gap narrowing, Hurkx and Shockley–Read–Hall (SRH) recombination, the concentration and field dependent mobility and trap-assisted-tunneling.

3. PROPOSED STRUCTURE

Figure. 1 illustrates a schematic view of the conventional III-V TFET and III-V TFET structure with source and channel heterojunctions, respectively. The body thickness and channel width are

both 10 nm. The channel length is 30 nm. Aluminum is used to form the gate electrode with work function of 4.2 eV and ZrO_2 is applied to the gate insulator with permittivity of $29\epsilon_0$. The gate oxide is 2 nm. In III-V TFET structure with source and channel heterojunctions, the channel is made from a 3 nm InAs layer and a 12 nm InAsAlSb layer with doping density of $1 \times 10^{16} \text{ cm}^{-3}$. In addition, the source are made from a 1.2 nm AlGaSb layer and a 3.3 nm GaSb layer with doping density of $5 \times 10^{19} \text{ cm}^{-3}$. The drain are made from 10 nm InAsAlSb layer with doping density of $2 \times 10^{19} \text{ cm}^{-3}$. On the other hand, the added heterojunctions in the channel and source are InAs/InAsAlSb and AlGaSb/GaSb layers, respectively.

4. RESULTS AND DISCUSSION

Figure. 2 shows gate voltage dependence of logarithm scaled drain current for the conventional III-V TFET and III-V TFET structure with source and channel heterojunctions with gate length of 30 nm biased at drain voltage of 1 V. It can be seen that by introducing with source and channel heterojunctions, III-V TFET structure with source and channel heterojunctions has a higher on-state current around 1 decade about 10^{-3} while maintaining off-state current of 10^{-13} , resulting in higher on-current/off-current ratio of 10^{10} as compared to conventional III-V TFET. Because of

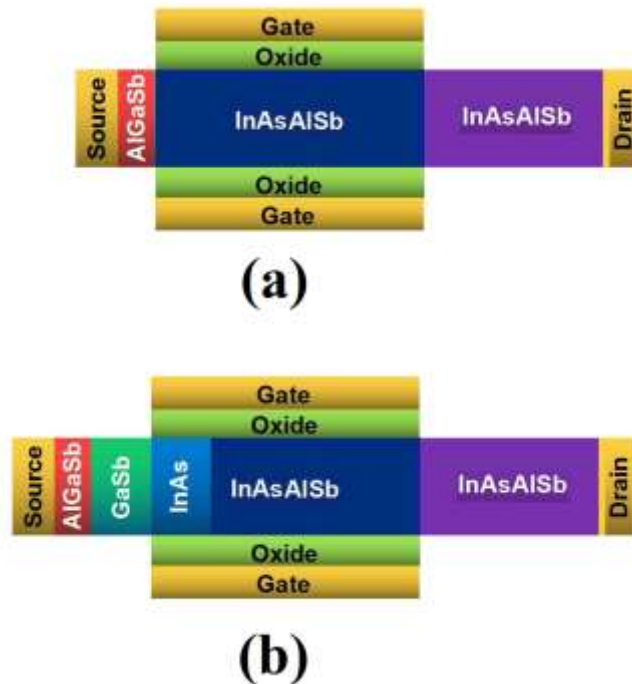


Figure 1: Schematic view of (a) the conventional III-V TFET and (b) III-V TFET structure with source and channel heterojunctions.

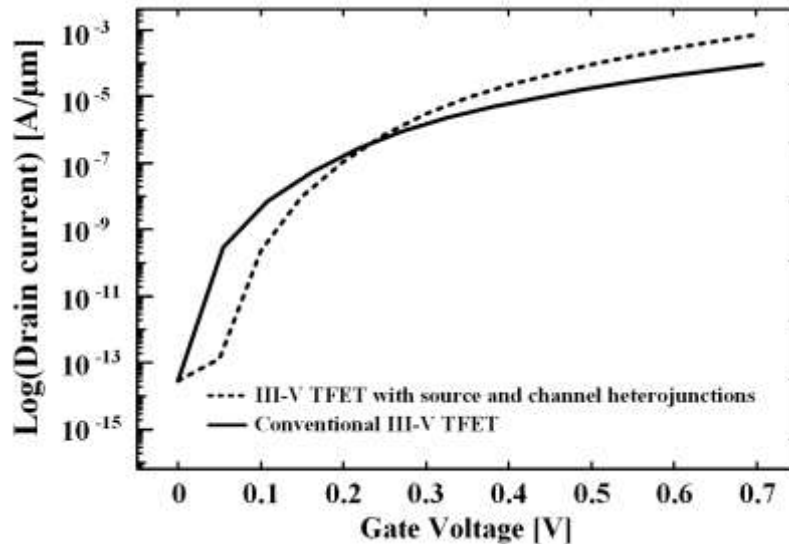


Figure 2: The gate voltage dependence of logarithm scaled drain current for the conventional III-V TFET and III-V TFET structure with source and channel heterojunctions.

two additional heterojunctions (one in the source and the other in the channel), the tunnel barrier height and tunnel distance significantly reduced. On the other hand, the low mass of an electron and bandgap in material of source and channel heterojunctions, the tunneling probability is increased. Therefore, the III-V TFET structure with source and channel heterojunctions has a higher drain current due to the increased tunneling probability. In addition, increased tunneling

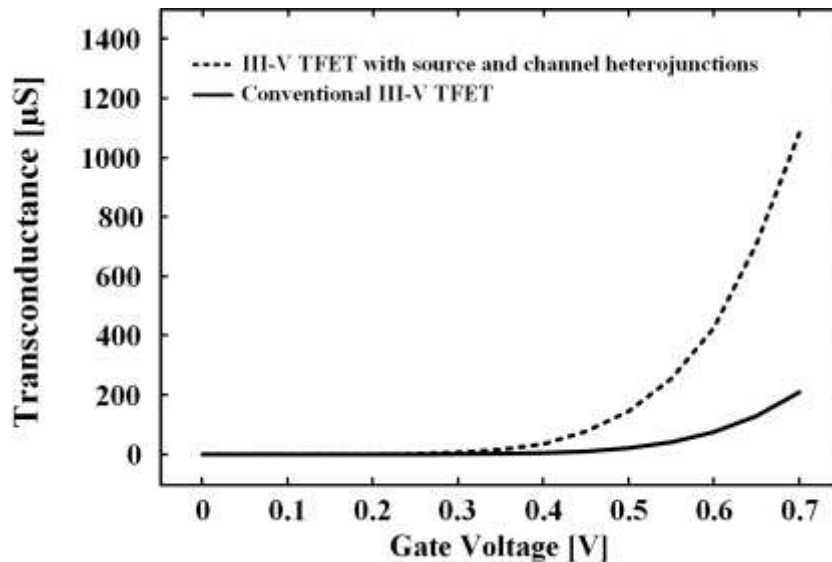


Figure 3: The gate voltage dependence of transconductances for the conventional III-V TFET and III-V TFET structure with source and channel heterojunctions.

probability induced by source and channel heterojunctions, causes smaller subthreshold-swing of 30 mV/decade can be achieved in the III-V TFET structure with source and channel heterojunctions in comparison with that of conventional III-V TFET.

Figure. 3 shows the comparison between the transconductances of the conventional III-V TFET and III-V TFET structure with source and channel heterojunctions with gate length of 30 nm biased at drain voltage of 1 V as a function of the gate voltage. As seen, the conductance of III-V TFET structure with source and channel heterojunctions increased by 450% at high gate voltage compared to that of the conventional III-V TFET because of the higher on-current.

In order to much better analysis of the performance parameters, the subthreshold slope was defined as the average slope between the off-state current and threshold current as below (Marjani, et al., 2016(b)):

$$SS = \frac{V_{th} - V_{off}}{\log \frac{I_{th}}{I_{off}}} \quad 11$$

where V_{th} is the threshold voltage and defined here by the constant current method at the point of 3×10^{-7} A/ μm , I_{off} is defined to be the drain current at onset gate voltage, while on-current is defined at gate voltage of 0.7 V. These definitions are used in the rest of this paper.

In order to investigate whether the source and channel heterojunctions effects were present when the feature size of the devices decreased, the performances of the III-V TFET structure with source and channel heterojunctions with different gate lengths were also examined. Except gate length, all factors are kept as similar in these simulations. Figure. 4 shows the performance comparison of the logarithm scaled on-current as a function of gate length for III-V TFET structure with source and channel heterojunctions at drain voltage of 1 V. It is evident that the on-current (tunneling from source to drain regions) increases as the gate length decreases from 90 to 15 nm.

Figure. 5 shows the comparison of the off-current as a function of gate length for III-V TFET with source and channel heterojunctions at drain voltage of 1 V. As can be seen, variation in off-current is the dominant as compared with on-current. It should be mainly because of short-channel effects such as DIBL and charge sharing induced by down scaling of gate length.

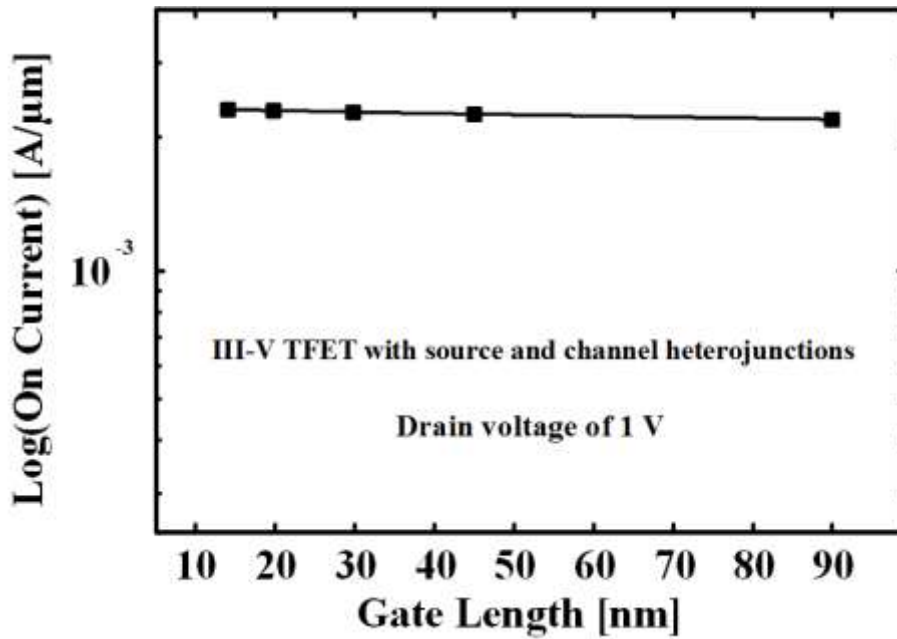


Figure 4: The gate length dependence of logarithm scaled drain current for the III-V TFET structure with source and channel heterojunctions.

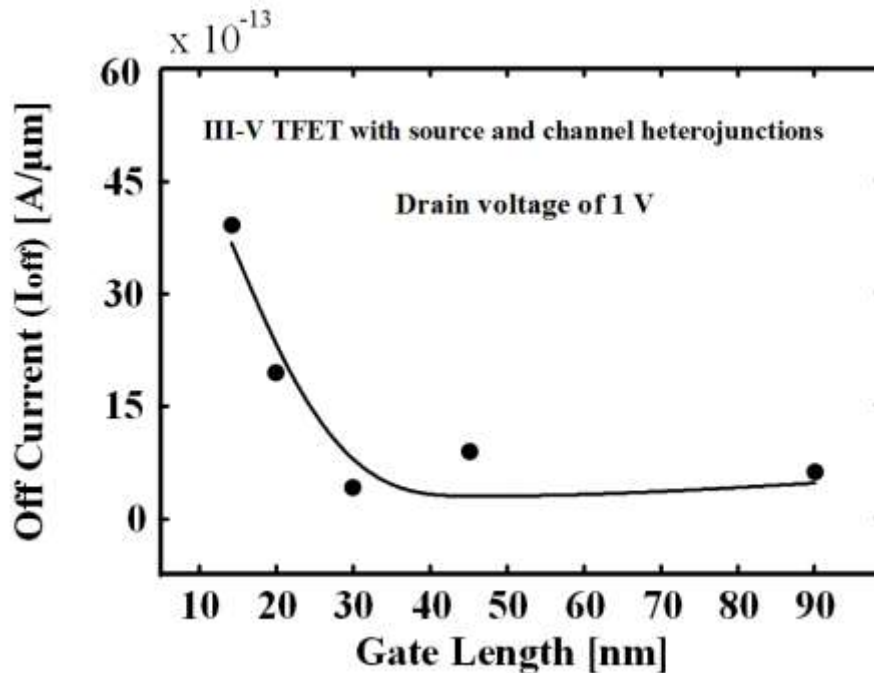


Figure 5: The gate length dependence of off-current for the III-V TFET structure with source and channel heterojunctions.

Figures. 6 and 7 show the plots for subthreshold-swing and on-current/off-current ratio as a function of different gate length for the III-V TFET structure with source and channel heterojunctions at drain voltage of 1 V, respectively. As can be seen, on-current/off-current ratio decreases and subthreshold-swing degrades with scaling down of gate length because of increasing off-current, as observed in Figure. 5.

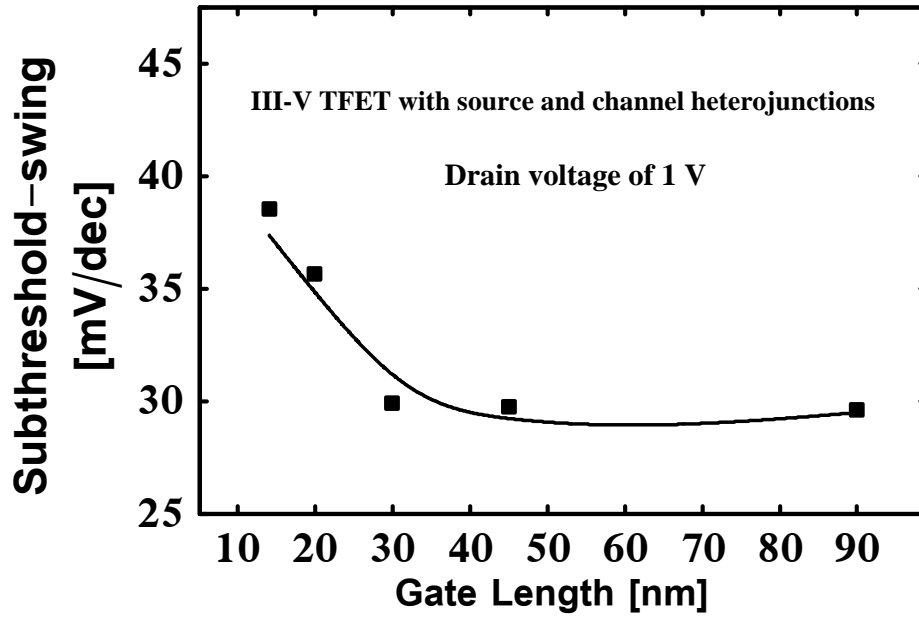


Figure 6: The gate length dependence of subthreshold-swing for the III-V TFET structure with source and channel heterojunctions.

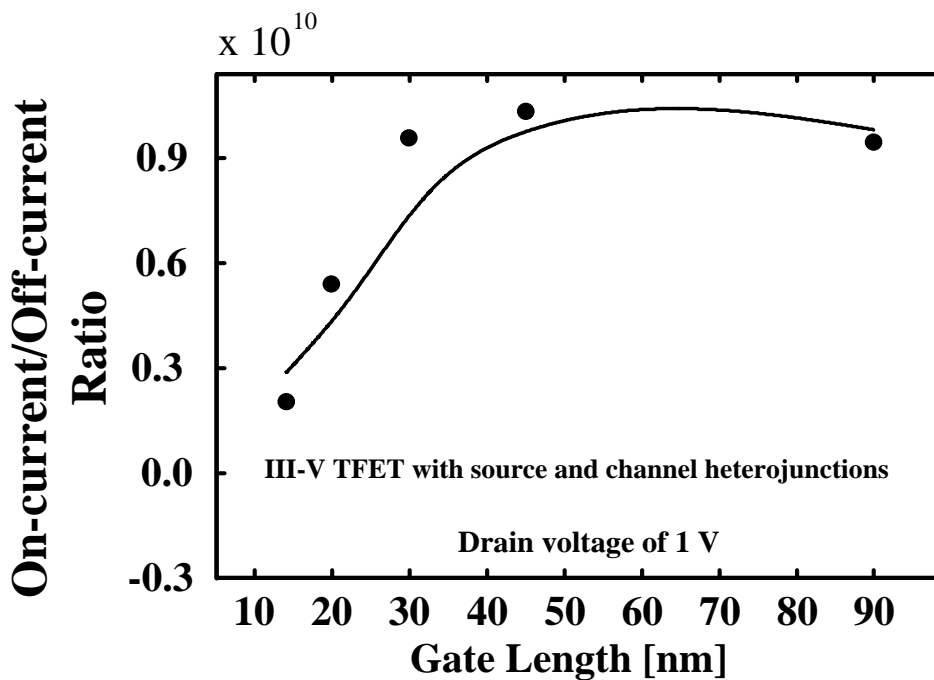


Figure 7: The gate length dependence of on-current/off-current ratio for the III-V TFET structure with source and channel heterojunctions.

5. CONCLUSION

In this work, a detailed study of the III-V tunneling field-effect transistor (TFET) with source and channel heterojunctions is reported and introduced. The proposed structure is combination

of the high tunneling efficiency induced by heterojunction material and the high mobility of III-V material. The III-V TFETs with source and channel heterojunctions have both shorter tunneling distance and two transmission resonances as compared to conventional III-V TFETs, that significantly improve the on-current. Furthermore, the transfer characteristics affected by gate length were evaluated. The results show that on-current, off-current, and on-current/off-current ratio and subthreshold-swing of III-V TFETs structure with source and channel heterojunctions are about 10^{-3} A/ μm , 10^{-13} A/ μm , 10^{-10} and 30 mV/decade, respectively.

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