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DC ANALYSIS OF p-n-p-n TUNNELING FIELD-EFFECT TRANSISTOR BASED ON $In_{0.35}Ga_{0.65}As$

B. DOROSTKAR*, S. MARJANI**
Electrical Engineering Department, Iran University of Science and Technology, Tehran, Iran
Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
behnamdorostkar@gmail.com*, saeid.marjani@mail.um.ac.ir**

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ABSTRACT

Using calibrated simulations, we report the $In_{0.35}Ga_{0.65}As$ based tunnel field-effect transistor (TFET) with thin δ-doped n^+ pocket at the source-channel interface to improve the parameters such as on current (I_{on}), off-current (I_{off}) and subthreshold swing (SS). The simulations results of proposed device is compared with analytical model that is shown with high precision of DC parameters by examining the effects of III-V semiconductor materials. Furthermore, the influence of pocket doping, pocket width, doping level, effective oxide thickness (EOT), temperature and mole fraction of III-V semiconductor material on device performance have been investigated. The results show that proposed device has a higher ON current (1×10^{-5} A/μm) and a steeper subthreshold swing (35 mV/decade) as compared with the conventional TFET. It shows a lot of promise for future scale CMOS technology for low voltage and high frequency application.

KEYWORDS: Analytical model, semiconductor materials, Tunneling field-effect transistor, ON current, OFF current.

1. INTRODUCTION

In the recent years, increasing utilization of portable device and wireless communication system caused ultralow power and high speed circuit to be interested under focus of which including SRAM, operational transconductance amplifiers (OTAs), analog to digital convertor(ADC) and current mode logic applications (marjani, et al., 2017; Bi, et al., 2017). It is clear that MOSFET is limited in subthreshold swing (SS) (60 mV/decade at room temperature) in recent technology (nanoscale system design) So tunnel field-effect transistor (TFET) is considered the best substitute for conventional CMOS (Zhao, et al., 2011). Enhance the current and steep subthreshold swing (below 60 mv/decade) are reliable trait as compared with MOS technology in ultralow voltage and high frequency applications (Vallett, et al., 2010; Ionescu and Riel, 2011). The method of carrier relocation is band-to-band tunneling (BTBT) (Zhu, et al., 2013) model which this phenomena betide between the source region and the channel region (Khayer and Lake, 2009). High ON current (I_{on}), low OFF current (I_{off}) and steep subthreshold swing are superior trait that make it distinguished from other devices. Also the biggest challenge is to design transistors that show simultaneously low threshold voltage and power consumption while maintaining reasonable current drivability. The silicon-based TFET exhibits a low sub-threshold swing and OFF current, but low ON current was controversial because of the low inter band tunneling (Guo, 2011). In order to achieve proper characteristics in terms of high I_{on} to I_{off} ratio and steep subthreshold swing, many structures have been suggested such as high-k dielectric materials (Boucart and Ionescu, 2007), pocket doping (Jhaveri, et al., 2011; Kao, et al., 2013; Chang, et al., 2013; Marjani and Hoseini, 2014a), double-gate (DG) TFET (Narang, et al., 2011), extended source (Marjani and Hoseini, 2015a), band gap engineering (Ganapath and Salahuddin, 2011) and multi gate structure (Marjani and Hoseini, 2015b). We can say several researchers have reported devices with SS below 60 mV/decade at room temperature in term of theoretically and experimentally (Brouzet, et al., 2015; Wu, et al., 2016; Marjani, et al., 2016b).

The III-V compounds have much lower effective masses, higher electron and hole mobility when compared with the silicon. Many structures in term of homo-junction and hetrojunction are design by low band gap materials, such as Germanium, Silicon-Germanium and Gallium Antimonide (GaSb) can be employed for source region, whereas, Indium Phosphide (InP) can be used as a high band gap material for drain and channel region (Low, et al., 2016).

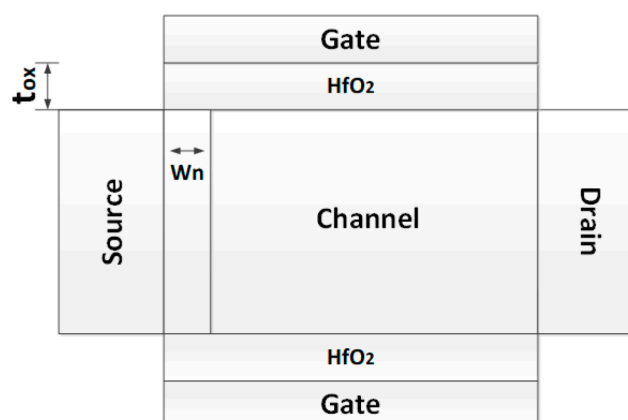

Figure 1: The schematic structure of double gate $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET.

In this paper, TFET with a δ-doped n^+ region at the source side with III-V compound semiconductors of $In_xGa_{1-x}As$ is proposed and evaluated. Also, the proposed structure is optimized in term of pocket parameters. The rest of paper is organized as follows: In section 2, we describe the device proposed structure based on group III-V semiconductor materials and analytical model will be analysed. Section 3 show the DC analyses for the proposed TFET, the conclusions can be seen in section 4.

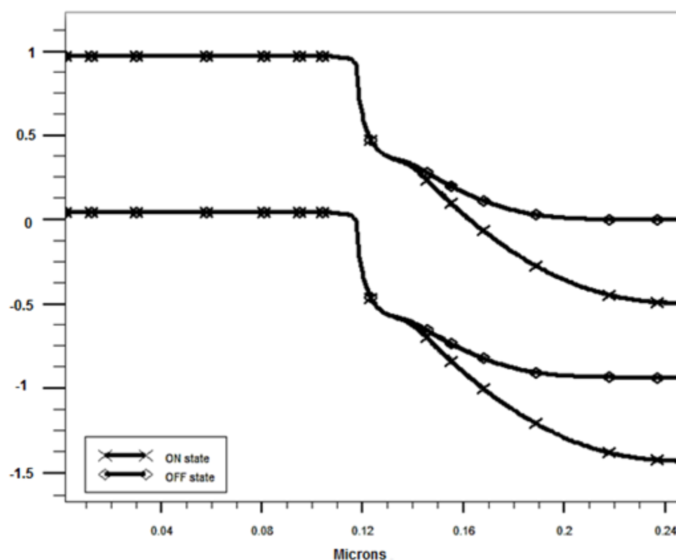

Figure 2: Simulated energy band diagram of proposed device in the off-state and the on-state

2. ANALYTICAL MODEL AND DEVICE STRUCTURE

The energy band diagram along the horizontal direction under the oxide-silicon interface is shown in Figure 2 for the off-state (V_{GS} = 0 V and V_{DS} = 1 V) and the on-state (V_{GS} = V_{DS} = 1 V) of 20 nm channel length $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET. Since the p and n regions are degenerately Boltzmann's approximation cannot accurately describe carrier statistics in these regions.Therefore,expressions for potiontial barrier use the approximation of Fermi–Dirac distribution. In the channel region the expression for the electric field is (Gholizadeh and Hosseini. 2014):

$$\varepsilon\left(x\right)=\frac{1}{\varepsilon}\int\rho dx \qquad 1$$

where ρ is the charge density. For p-n-p-n structre, the expression described as (Hosseini and Moghaddam, 2015; Marjani and Hoseini, 2015c):

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$$\varepsilon(x)=\begin{cases}\frac{qN_S}{\varepsilon_S}(X_P+X) & -X_P\langle X\langle 0\\ \frac{qN_SX_P}{\varepsilon_S}+\frac{qN^+}{\varepsilon_S}X & 0\langle X\langle W\\ -\frac{qN_SX_P}{\varepsilon_S}+\frac{qN^+W}{\varepsilon_S}+\frac{qN_I}{\varepsilon_S}(-W+X) & W\langle X\langle W+L\\ -\frac{qN_SX_P}{\varepsilon_S}+\frac{qN^+W}{\varepsilon_S}-\frac{qN_IL}{\varepsilon_S}+\frac{qN_D}{\varepsilon_S}(X-(W+L)) & W+L\langle X\langle W+L+X_N\end{cases} \quad 2$$

Depletion region lengths in p and n regions are x_p and x_n, respectively. The band-to-band tunneling rate and the tunneling current in junction region can be gained by (Marjani, et al., 2016a):

$$G_{BTBT}=\frac{q^2\sqrt{m_r^*}}{2\pi h^2E_g^{0/5}}E^2.exp\left(\frac{-\pi\sqrt{m_r^*}Eg^{\frac{3}{2}}}{2qhE}\right)\Delta\phi \quad 3$$

In which m^* is the electron effective mass, Eg and $\Delta\phi$ are the band gap and energy range in the tunneling region length, respectively *E* is total electric field at the tunneling junction.

$$1/m_r^*=1/m_h^*+1/m_e^* \quad 4$$

where m is effective mass. The source drain tunnel current of pnpn TFET is given by (Hosseini and Moghaddam, 2015):

$$I_{DS}=q\int G_{BTBT}dv \quad 5$$

where V is the three-dimensional device volume where tunnel paths start. We indicate that analyticaly drain current and the simulation based drain current closely match.

Figure 1 shows the cross sectional view of of proposed structure with channel length of 20 nm. The source and drain of conventional TFET structure are regions with high doped. The proposed structure is $In_xGa_{1-x}As$ based p-n-p-n TFET that the tunneling junction is formed between the source and n-pocket that helps to reduce the tunneling width and thus improves the Ion and SS. One requirement to achieve optimum TFET performance is a low effective energy barrier for band-to-band tunneling and a small effective mass of the charge carrier. Therefore, structures based on all-III–V materials are very attractive because their effective bandgap can be engineered. The simulated device has a intristic channel doping concentrations of 5× 10^{15} cm^{-3} with a 20 nm channel length. The drain region is n^+ with doping concentration of 2×10^{18} cm^{-3} and the source region with doping concentration of 2×10^{20} cm^{-3}. This asymmetrical doping profile between the source and drain regions is commonly used for reducing ambipolar effects. Also, in order to improve the gate control, double gate structure is employed. The gate oxide thickness is 3nm and work function of the metal gate is 5.3 eV. The high-k dielectric materials (HfO_2) is used to improveing the Ion and hence achieve high on to off current ratio. the drain voltage is set 1 V for low voltage applications.

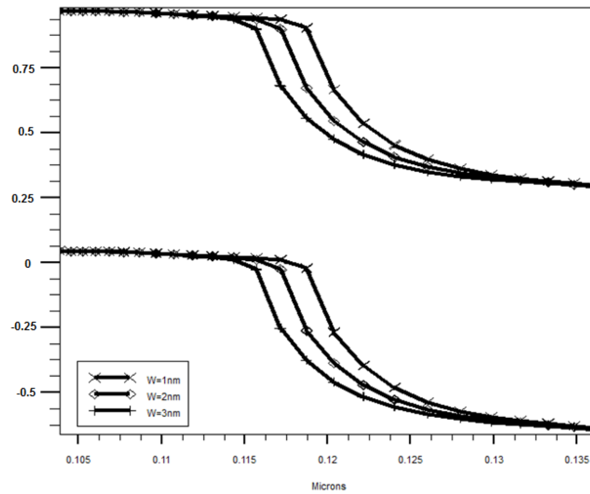

Figure 3: The energy band diagram of $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET with different Wn.

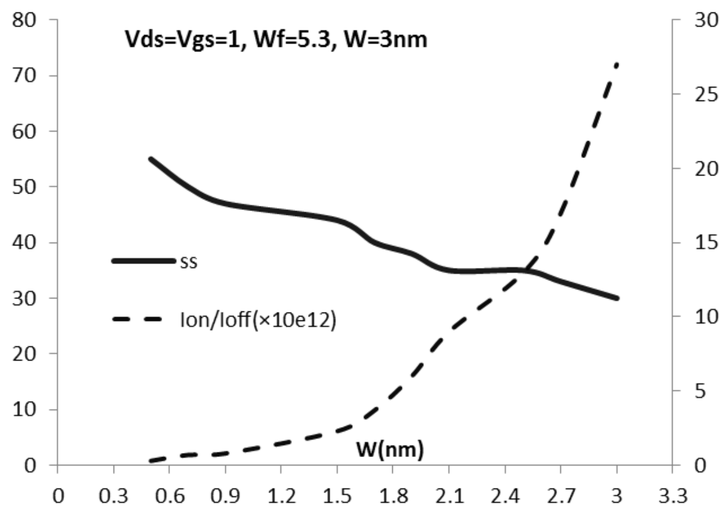

Figure 4: Ion/Ioff and SS of $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET as a function of Wn.

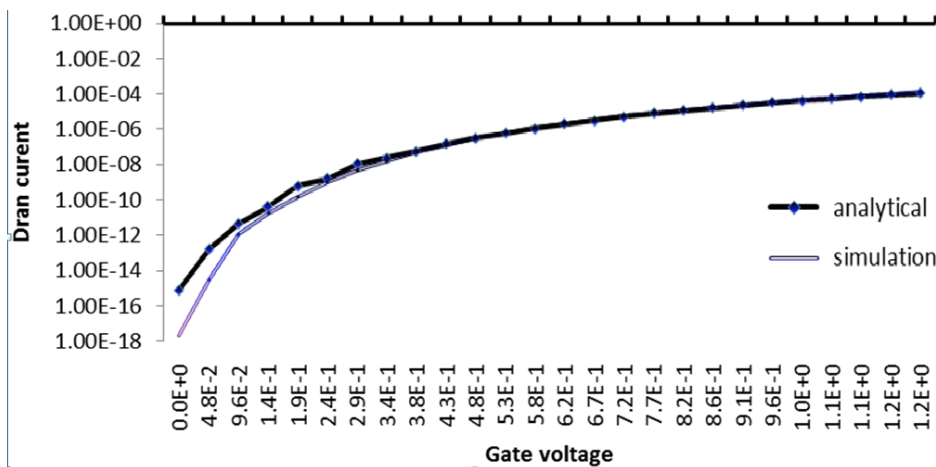

Figure 5: I_{DS}-V_{GS} of $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET with 20 nm of channel length and 3 nm of pocket width in simulation and analytical.

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3. RESULTS AND DISCUSSION

Silvaco TCAD software (Atlas, 2010) was adopted for the simulation of proposed structure. In this simulation tool, a uniform doping profile is used for all regions. Due to the unique characteristics of the TFETs some models have been used including nonlocal band-to-band tunneling, concentration and field dependent mobility, generation and recombination and band gap narrowing (Marjani and Hoseini, 2015a ; Marjani and Hoseini, 2014b; Marjani and Hoseini, 2014c).

Base of TFET structure is gate controlling. The gate is able to control the tunneling barrier width. With $V_{GS} = V_{DS} = 1$ V in the ON state, the gate leading significant band to band tunneling of electrons from the valance band of the source to the conduction band on the channel. In the OFF state, tunneling length is not sufficient for the tunneling; as a result of that a small current flow across the device.

In this part, we investigate the device based on $In_{0.35}Ga_{0.65}As$. The tunneling probability depends on the pocket width (Wn) extremely. energy band diagram of proposed device (ON state) with different pocket is shown in Figure 3. on-curren will be improve with decreasing pocket width. In Figure 4, the dependence of Ion/Ioff and SS on the pocket width are shown. It is clear that pocket width is optimized around 3 nm and both Ion/Ioff and SS are in the best condition.

Figure 5 display the input characteristic of the proposed device in the simulation and the analytical model that helps to find the OFF current and SS in the sub-threshold region. The analytical model is validated via numerical results obtained from device simulations based on non-local band-to-band tunneling model. It is clearly that the values of Ion and Ioff are around 1×10^{-5} A/μm and 1×10^{-18} A/μm. Figure 6 display the effect of gate oxide thickness on the drain current and sub threshold swing of proposed TFET. It is clearly seen that for small gate oxide thickness, the tunneling current is higher as depicted in figure 6.

Figure 7 shows I_{on}/I_{off} and SS for the $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET with 20 nm gate length and 3 nm of pocket width as a function of the temperature at $V_{GS} = V_{DS} = 1$ V. As can be seen, the off-current increases 4 order at high temperature because of thermal generation of carrier in depletion region. It decreases I_{on}/I_{off}, however the variation of temperature is slight effect on the subthreshold swing.

Different levels of p-doping for the source region and n-doping for the drain region are shown in Figure 8. The source doping has a high impact on the on-current level, since the tunneling takes place between the source and the intrinsic region. The highest-possible source doping is acceptable for optimized Tunnel FET operation. Lowering the drain doping lowers the OFF current and sub threshold swing.

In order to demonstrate the effect of mole fraction of $In_{0.35}Ga_{0.65}As$ material on the TFET performance, the energy band diagrams with different mole fraction are shown in Figure 9. It is observed, I_{on} is increase and BTBT mechanism has operated properly with mole fraction of 0.85. In this way, the values of I_{on} and I_{off} are around 1×10^{-5} A/μm and 1×10^{-18} A/μm, respectively at V_{DS} = 1 V. Therefore, value of I_{on}/I_{off} is 10^{12} that is remarkable. In addition, the minimum point subthreshold swing value is about 35 mV/decade. These results indicate that the $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET has improved device characteristics, including higher I_{on} and I_{on} /I_{off}; and a steeper subthreshold swing as compared with the conventional p-i-n TFET.

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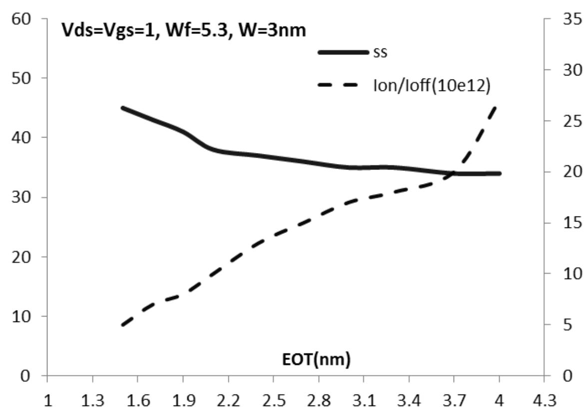

Figure 6: Variation of Ion/Ioff and SS for different gate oxide thicknesses.

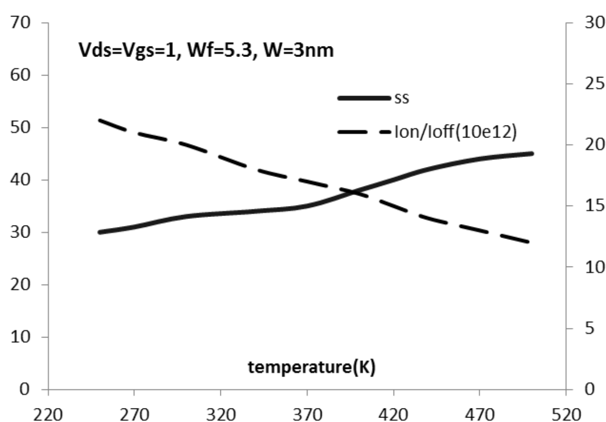

Figure 7: I_{on}/I_{off} and SS of $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET for various temperatures.

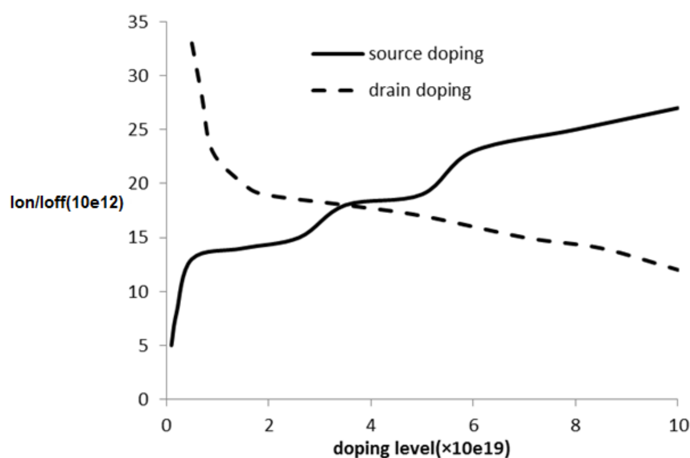

Figure 8: I_{on}/I_{off} of the $In_{0.35}Ga_{0.65}As$ p-n-p-n TFET with 20 nm gate length and 3 nm of pocket width as a function of the doping concentrations of the source and drain region at $V_{GS} = V_{DS} = 1$ V.

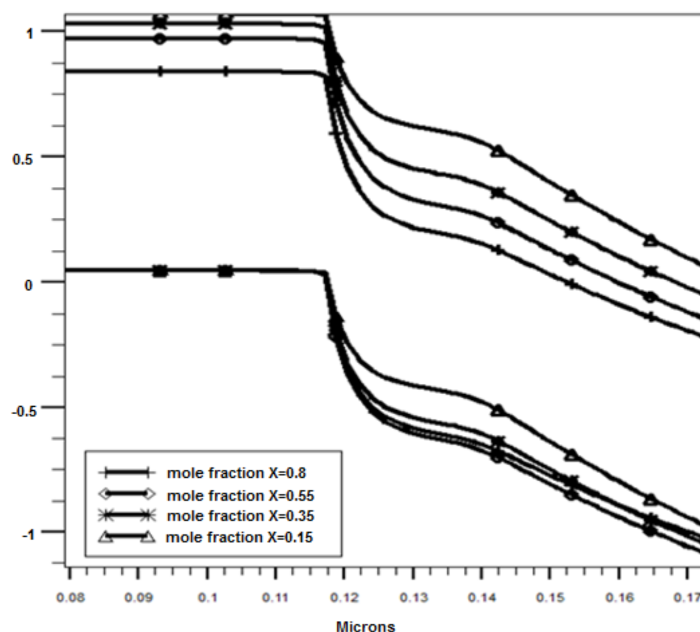

Figure 9: The energy band diagram of $In_xGa_{1-x}As$ p-n-p-n TFET with different mole fraction.

Table.1: The extracted result of $Al_{0.35}Ga_{0.65}As$ p-n-p-n TFET.

structure / parameter	TFET based on III-V
Subthreshold swing (mV/decade)	35
I_{on} (A/µm)	2×10^{-5}
I_{off} (A/µm)	3.5×10^{-18}
V_{th} (V)	0.23
Triode slope (mV/decade)	19.5
Saturation slope (mV/decade)	0.13

4. CONCLUSION

This paper presented the p-n-p-n TFET based on $In_{0.35}Ga_{0.65}As$ as III-V semiconductor material for further increase both the I_{on} /I_{off} ratio and subthreshold swing of device. Also, an analytical model is presented for the potential distribution and the drain current of proposed device. The proposed analytical model is validated via numerical results obtained from device simulations based on calibrated nonlocal band-to-band tunneling model. The proposed structure has p^+-i-n^+ structure with a thin δ-doped n^+ pocket at the source-channel interface, low band gap, small tunneling mass, and different band-edge alignment induced by the group III-V semiconductor. The results show that $In_{0.35}Ga_{0.65}As$ based p-n-p-n TFET shows a higher Ion and steeper subthreshold swing as compared with the conventional p-i-n TFET that is expected to be a promising candidate for ultralow power applications and switching devices.

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